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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/395,294 | 09/13/1999 | SOPHIE WILSON | 1073/OG117 | 5796 |

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| EXAMINER |
|---|
| MEONSKE, TONIA L |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 18 |

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/395,294 | WILSON, SOPHIE | |
| | Examiner | Art Unit | |
| | Tonia L Meonske | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,4-12 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4, 7, and 8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shiell et al., US Patent 6,317,820, cited as prior art reference in paper number 6, mailed on January 15, 2002.

3. The rejections to claims 4, 7, and 8 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 16, mailed on April 3, 2003.

*4.* Furthermore, claim 1 was amended to further recite cancelled claims 2 and 3 which were also clearly anticipated by Shiell et al. explained in the prior office action, therefore the rejection to claim 1 is respectfully maintained and incorporated by reference set forth in the last office action for rejections to claims 1, 2, and 3, in paper number 16, mailed on April 3, 2003.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in. which the invention was made.

6. Claims 5, 6, 9, 10, 11, 12, 14, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, cited as prior art reference in paper number 6, mailed on January 15, 2002, in view of Yoshida, US Patent 5,761,470.

7. The rejections to 5, 6, 9, 10, 11, and 14 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 16, mailed on April 3, 2003.

8. Furthermore, currently amended claims 12 and 15, merely added limitations already present in claim 8, and therefore currently amended claims 12 and 15 are rejected for the same reasons as recited in claims 8, 12, and 15, of paper number 6, mailed on January 15, 2002.

9. Furthermore, some limitations in claim 16 were deleted, and claim 16 was amended to be dependent from claim 12. Therefore, claim 16 is now rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, in view of Yoshida, US Patent 5,761,470, for the reasons as set forth with respect to claims 8 and 12 in the last office action, paper number 16, mailed on April 3, 2003.

***Response to Arguments***

10. Applicant's arguments filed July 3, 2003 have been fully considered but they are not persuasive.

11. On page 8, Applicant argues in essence:

> *"The instruction format and decode unit are configured such that the claimed computer system can execute single operations or dual operations, each employing the resources of the computer differently, based on the identification bits within the instruction (see ID1 and ID 2 in Figs. 2a and 2b). As a consequence, only one decode unit and one set of instructions bit per predetermined bit length is needed. This drastically simplifies the fetch and decode instruction semantics requires to achieve a given level of performance, while retaining the capability of selecting between levels of instruction parallelism. This novel feature of the invention is reflect in all of the independent claims and is not disclosed in any of the presently cited prior art documents."*

However, since the claims do not define how the "detection" occurs, any manner of detecting single vs. dual operation instructions will read upon the claims.

Shiell et al. in combination with Yoshida have taught that the instruction format and decode unit are configured such that the claimed computer system can execute single operations or dual operations, each employing the resources of the computer differently, based on the identification bits within the instruction. Shiell et al. have taught that the instruction format and decode unit (Figure 1, element 115) are configured such that the claimed computer system can execute single operations (column 2, lines 25-30) or dual operations (column 2, lines 30-52), each employing the resources of the computer differently (Column 2, lines 26-37, in the single operation mode, instructions are executed by selected ones of the functional units, under control of a predetermined program counter. In the dual operation mode, a first program counter controls execution of program instructions using a first group of data registers and a first group of functional units, and a second program counter controls execution of program instructions using a disjoint second group of data registers and a disjoint second group of functional units.) Shiell et al. have not specifically taught that this is based on the identification bits within the instruction. Yoshida has taught each instruction of said predetermined bit length includes a set of identification bits at designated bit locations within the instruction (Figure 25, elements 505 and 506), said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction (Figure 25, Figure 26, FM). It would have

been obvious to one of ordinary skill in the art at the time the invention was made to have each instruction of Shiell et al. contain a set of identification bits at designated bits at designated bit locations within the instruction, as taught by Yoshida, in order to easily determine whether the instruction is a long instruction or a dual instruction operation. Having the designated bits at predetermined bit locations within the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the code of execution of the instruction. Therefore this argument is moot.

12. On pages 9, 10, and 11, Applicant argues in essence:

*"However, Sheill et al. fail to teach the limitations the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and a second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously," and the "instruction defines two independent operations, supplying one of the operation of the first processing channel and the other one of the operations to the second processing channel whereby the operations are executed simultaneously," as set forth in amended independent claims 1, 12, and 15 and method claim 8, respectively. Here the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself. "*

However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself) are not recited in the rejected claims 1, 12, and 15. Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore Shiell et al. has in fact taught "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations (column 2, lines 23-56, Second mode), it is operable to control the first channel to implement one of those operations (column 2, lines 23-56, A side operation) and a second channel to implement the other of those operations (column 2, lines 23-56, B side operation), whereby the first and second channels execute their respective independent operations simultaneously (column 2, lines 23-56)," and the "instruction defines two independent operations, supplying one of the operation of the first processing channel and the other one of the operations to the second processing channel whereby the operations are executed simultaneously (column 2, lines 23-56),".

Therefore this argument is moot.

13. On page 11, Applicant argues in essence:

*"Applicant respectfully asserts that although Yoshida discloses bits within an instruction, it is only for use by a single channel processor. It follows that this reference also fails to teach two channels that operate either independently or in cooperation with each other."*

However, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, Yoshida was not cited for teaching two channels that operate either independently or in cooperation with each other. Therefore the fact that Yoshida has not

taught the two channels is not relevant to the rejection, because Shiell et al. have taught these features, see above arguments.

***Conclusion***

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

18. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
September 17, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER